Parallel LVDS Front-End

MULTI-CHANNEL DATA RECEPTION & GENERATION

The Parallel LVDS Front-End (PLFE) provides multi-channel data reception and generation capabilities with rates of up to 2Gbps per channel. The PLFE provides up to four 8-bit or two 16-bit parallel data busses in both directions (reception and generation). The PLFE is part of the suite of latest generation EGSE products from Celestia STS.

The PLFE operates as the electrical interface towards flight equipment and can be used on all AIT levels (module, unit, instrument, panel and satellite).

The PLFE provides the electrical, data extraction, protocol handling and status annotation functions . The recovered data (or data to be generated) is offloaded from the PLFE using a 10Gbit TCP/IP streaming interface (SFP+, optical or copper) to a commercial server platform for data storage (or replay) to local disks (SSD or HDD).

KEY FEATURES

General

- Modular Implementation
- Gigabit LAN for Control and Monitoring via TCP/IP (via RJ45)
- 10Gbit LAN for Data Streaming via TCP/IP (via SFP+)
- External PPS input for time synchronisation
- Post-processing of received data with C-STS Level-0 Processing Software (LZP)

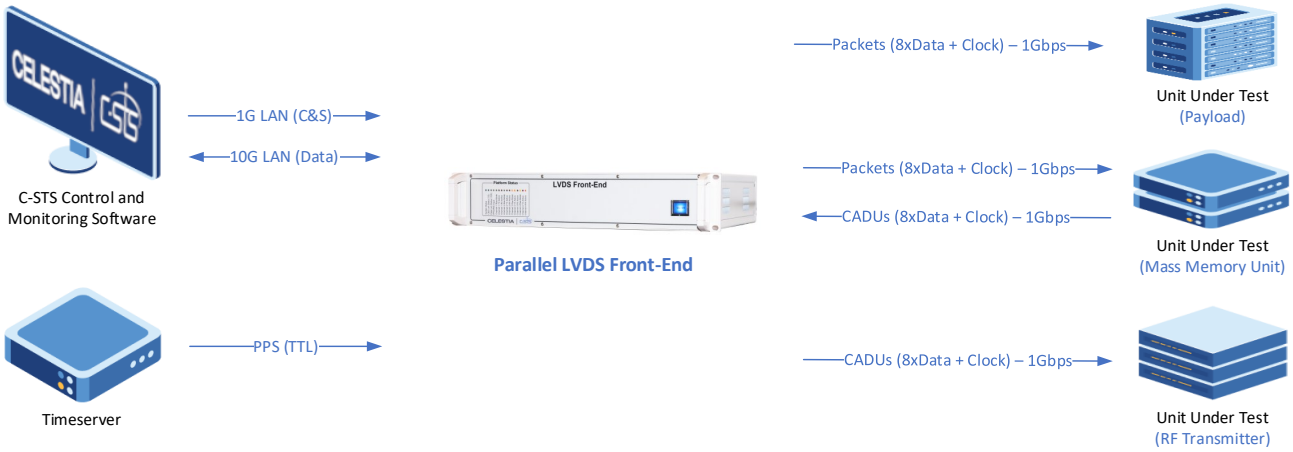
Parallel LVDS Inputs & Outputs

- Up to 4 Parallel LVDS Inputs and Outputs (8-bits Data and Clock) in parallel
- Teaming of 2 channels to 16-bit Parallel Interfaces
- Optional LVDS Flow Control and Data Enable signals for all Channels supported
- Input clocking in excess of 125MHz
- Output Clock programmable in excess of 125MHz in 1Hz steps
- Input and Output Data Bandwidths:
    - 8-bit Parallel > 1Gbps per channel
    - 16-bit Parallel > 2Gbps per channel
- All LVDS I/O's are Electrically Isolated from Chassis/Safety Ground
- Standard HDD26 Female Connector for each Input and Output Channel
- TIA/EIA-644-A Compliant LVDS Interfaces
- Hardware timestamping of received data blocks
- Timed acquisition of data and release of data for transmission
- All interfaces are FMEA compliant.

EXAMPLE APPLICATIONS

- Instrument / Payload Data Acquisition and/or Simulation
- Mass Memory Unit Testing and/or Simulation
- Laser Communication Terminal (LCT) Interfaces

PARALLEL LVDS FRONT-END



The PLFE parallel LVDS inputs and outputs supports up to four 8-bit data + clock interfaces in parallel, where the clock for each channel can run in excess of 125MHz. In addition it is possible to team two channels to operate as a single 16-bit data + clock interface. Supports flow-control and enable signals.

All LVDS in- and outputs are fully isolated (with respect to the chassis/safety ground) and provide satellite level fault voltage emissions and tolerances.

The unit is provided with an Failure Mode and Effects Analysis (FMEA) report.

DATA STORAGE INTERFACE

The back-end interface is implemented using a low-latency 10G TCP/IP and MAC implementation directly within the hardware, capable of providing >9Gbps sustained data streaming bi-directional. This provides back-end independence, allowing commercial servers with standard 10G ethernet cards to be used. The PLFE is delivered with back-end software (Windows Server) for data storage and replay as well as Archive Browser software for visualising and exporting recorded data.

ENVIRONMENTAL AND PHYSICAL SPECIFICATIONS

Dimensions (H x W x D)	88.9mm x 435mm x 400mm
Weight	5.3kg
Input Power Range	100-240VAC 50-60Hz
Max Power Consumption	180W
Operating Temperature Range	+10°C to +40°C
Operating Humidity	30% to 85% (non-condensing)
Storage Temperature	-20°C to +60°C
Storage Humidity	Up to 85% (non-condensing)

www.celestia-sts.com | +31 717515100 | info@celestia-sts.com
Celestia STS, Mendelweg 32, 2333 CS, Leiden The Netherlands

Scan the QR code to access the C-STS website for all data sheets and more information